PLEASE AMEND THE CLAIMS AS FOLLOWS:

1. (Currently amended) A configuration method of interconnects of a chip, the chip having a power bus, a first metal layer and a plurality of electronic circuits, wherein the first metal layer has a plurality of power lines, and the power lines are substantially parallel and ~~electrically~~ connected to the power bus, the configuration method comprising:

generating a mask pattern of a plurality of metal lines of a second metal layer with an automatic place and route process for interconnection of said electronic circuits with at least one sparse area formed on the second metal layer; and

generating another mask pattern of at least one supply-power area in the sparse area and providing connection path from the supply-power area to the power bus, wherein the supply-power area has a plurality of metal-line associated slot areas, and each said slot area contains a pattern of at least one of the metal lines.

2. (Currently amended) The configuration method of claim 1, wherein the supply-power area is connected to one of the power lines with at least one via plug, whereby the supply-power area is connected to the power bus indirectly.

3. (Original) The configuration method of claim 1, wherein the supply-power area is connected to the power bus directly.

4. (Original) The configuration method of claim 1, wherein the supply-power area is directly merged with the power bus.

5. (Currently amended) The configuration method of claim 1, wherein at least one spacing is between the supply-power area and the metal lines pattern.

6. (Original) The configuration method of claim 5, wherein the spacing is not less than a minimum dimension, and the minimum dimension complies with a design rule for unrelated metal-to-metal spacing.

7. (Original) The configuration method of claim 1, wherein the supply-power area is a solid metal area.

8. (Original) The configuration method of claim 1, wherein the supply-power area is a non-solid metal area.

9. (Original) The configuration method of claim 1, wherein the supply-power area is a mesh-like metal area.

10. (Currently amended) The configuration method of claim 2, wherein when a quantity of the via plugs vertical to the first metal layer is plural, and the via plugs are directly stacked to connect ~~electrically~~ the supply-power area and one of the power lines.

11. (Ccurrently amended) The configuration method of claim 2, wherein when a quantity of the via plugs vertical to the first metal layer is plural, the via plugs are indirectly stacked to connect the supply-power area and one of the power lines.

12. (Currently amended) The configuration ~~manufacturer~~ method of claim 1, wherein when a quantity of the second metal layers is two, positions of the two supply-power areas on the two second metal layers substantially correspond to each other with overlapping to form a capacitor.

13. (Currently amended) An interconnection structure of a chip, wherein the chip has a power bus and a plurality of electronic circuits, the interconnection structure comprising:

a first metal layer having a plurality of power lines, wherein the power lines are substantially parallel and electrically connected to the power bus; and

at least one second metal layer having a plurality of metal lines and at least one supply-power area, wherein the metal lines are formed by an automatic place and route process for interconnection of said electronic circuits, and at least one sparse area is formed on the second metal layer, the supply-power area is formed in the sparse area and electrically connected to the power bus, and the supply-power area has a plurality of metal-line associated slot areas, and each said slot area contains at least one of the metal lines.

14. (Original) The interconnection structure of claim 13, wherein the supply-power area is electrically connected to one of the power lines with at least one via plug, whereby the supply-power is electrically connected to the power bus indirectly.

15. (Original) The interconnection structure of claim 13, wherein the supply-power area is electrically connected to the power bus directly.

16. (Original) The interconnection structure of claim 13, wherein the supply-power area is directly merged with the power bus.

17. (Original) The interconnection structure of claim 13, wherein at least one spacing is located between the supply-power area and the metal lines.

18. (Original) The interconnection structure of claim 17, wherein the spacing is not less than a minimum dimension, and the minimum dimension complies with a design rule for unrelated metal-to-metal spacing.

19. (Original) The interconnection structure of claim 13, wherein the supply-power area is a solid metal area.

20. (Original) The interconnection structure of claim 13, wherein the supply-power area is a non-solid metal area.

21. (Original) The interconnection structure of claim 13, wherein the supply-power area is a mesh-like metal area.

22. (Original) The interconnection structure of claim 14, wherein when a quantity of the via plugs vertical to the first metal layer is plural, the via plugs are directly stacked to connect electrically the supply-power area and one of the power lines.

23. (Original) The interconnection structure of claim 14, wherein when a quantity of the via plugs vertical to the first metal layer is plural, the via plugs are indirectly stacked to electrically connect the supply-power area and one of the power lines.

24. (Currently amended)The interconnection structure of claim 13, wherein when a quantity of the second metal layers is two, the positions of the two supply-power areas on the two second metal layers are substantially corresponding to each other with overlapping for forming a capacitor.